(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
15 February 2001 (15.02.2001)

PCT

(10) International Publication Number
WO 01/11766 A1

(51) International Patent Classification⁷: H03C 3/09

(21) International Application Number: PCT/US00/21016

(22) International Filing Date: 1 August 2000 (01.08.2000)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09/369,484 5 August 1999 (05.08.1999) US

(71) Applicant: RAYTHEON COMPANY [US/US]; 141 Spring Street, Lexington, MA 02173 (US).

(72) Inventor: GENRICH, Thad, J.; 18805 East Napa Drive, Aurora, CO 80013 (US).

(74) Agent: MEIER, Harold, E.; Baker Botts L.L.P., 2001 Ross Avenue, Dallas, TX 75201-2980 (US).

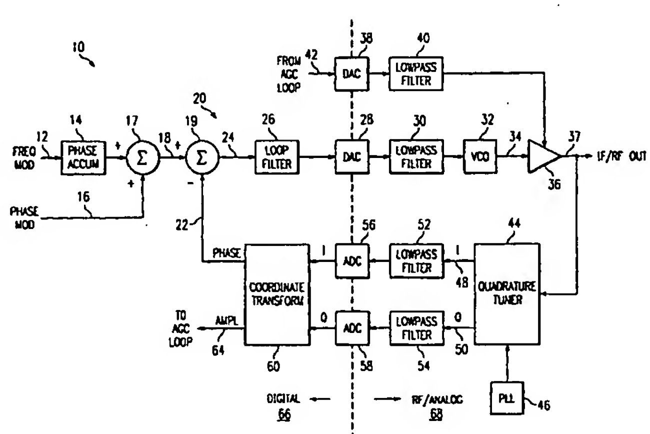
(81) Designated States *(national)*: AE, AG, AL, AM, AT, AT (utility model), AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CR, CU, CZ, CZ (utility model), DE, DE (utility model), DK, DK (utility model), DM, DZ, EE, EE (utility model), ES, FI, FI (utility model), GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KR (utility model), KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SK (utility model), SL, TJ, TM, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Published:
— *With international search report.*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: APPARATUS AND METHOD FOR PHASE AND FREQUENCY DIGITAL MODULATION



(57) **Abstract:** Apparatus for phase/frequency digital modulation includes a digital circuit receiving and processing a digital modulation input signal to generate a digital modulation control signal, a digital-to-analog converter coupled to the digital circuit converts the digital modulation control signal into an analog modulation control signal, and an RF/analog circuit is coupled to the digital-to-analog converter. The RF/analog circuit includes a voltage controlled oscillator to generate a modulated output signal in response to the analog modulation control signal, and a quadrature tuner coupled to the voltage controlled oscillator generates an in-phase tuner output and a quadrature tuner output in response to the modulated output signal. An analog-to-digital converter is coupled to the quadrature tuner and converts the in-phase tuner output and the quadrature tuner output to digital in-phase and quadrature tuner outputs. The digital in-phase tuner output and the quadrature tuner output are fed back to the digital circuit to generate the digital modulation control signal.

WO 01/11766 A1

APPARATUS AND METHOD FOR PHASE AND FREQUENCY DIGITAL MODULATION

TECHNICAL FIELD OF THE INVENTION

This invention is related in general to signal modulation, and more particularly, to apparatus and method for phase and frequency digital modulation.

BACKGROUND OF THE INVENTION

The typical digital phase and frequency modulator (PM/FM) suffers from one or more inherent performance and/or implementation limitations. One conventional approach for digital phase and frequency modulation first generates a relatively low frequency modulated signal using a low to moderate sample rate digital to analog converter (DAC) and an anti-aliasing filter. The resulting signal is then up-converted to the desired output frequency using one or more frequency translation circuits. The disadvantages of this approach are the complexity of the frequency translation circuit implementation using mixers and filters, isolation and bandwidth limitations associated with frequency translation filtering, and the presence of mixing spurious signals at the final output.

Another similar conventional implementation generates quadrature low frequency modulated signals using two digital-to-analog converters and anti-aliasing filters with a low to moderate sample rate. These signals are used to control a quadrature modulator, which directly produces the modulated output centered at the frequency of its local

oscillator input. This approach provides lower complexity and wider output bandwidth capabilities than the up-conversion approach. However, the major disadvantage of this approach is that it produces distortions due to amplitude and phase imbalances which are unacceptable in many applications.

A third conventional approach uses an undersampling (or bandpass sampling) technique with a digital-to-analog converter with a moderate to high sample rate. The output signal is a sampling image which is a sum or difference of the fundamental digital-to-analog converter output frequency and a harmonic of the sampling frequency. The image is selected from all of the other images present at the digital-to-analog converter output with a bandpass filter. This approach has bandwidth limitations due to the output filtering, and dynamic range (signal-to-noise ratio) limitations of the digital-to-analog converter at output frequencies above its sample rate.

A fourth conventional implementation utilizes a very high speed digital-to-analog converter which oversamples the desired output frequency. This approach avoids the frequency conversion and filtering limitations of the other aforementioned implementations. However, spurious signals are present in the output of this implementation due to the limited resolution of the high speed digital-to-analog converter. The high levels of the spurious signals are unacceptable in many applications. The circuitry required to generate the high speed digital-to-analog converter data inputs also generally has much higher complexity and power consumption than the other approaches.

SUMMARY OF THE INVENTION

It has been recognized that it is desirable to provide apparatus and method for phase and frequency digital modulation which avoids the problems and disadvantages of conventional circuits.

In one embodiment of the invention, apparatus for phase/frequency digital modulation includes a digital circuit receiving and processing a digital modulation input signal to generate a digital modulation control signal, a digital-to-analog converter coupled to the digital circuit operable to convert the digital modulation control signal into an analog modulation control signal, and an RF/analog circuit coupled to the digital-to-analog converter. The RF/analog circuit includes a voltage controlled oscillator operable to generate a modulated output signal in response to the analog modulation control signal, and a quadrature tuner coupled to the voltage controlled oscillator operable to generate an in-phase tuner output and a quadrature tuner output in response to the modulated output signal. An analog-to-digital converter is coupled to the quadrature tuner and operable to convert the in-phase and quadrature tuner outputs to digital in-phase and quadrature tuner outputs. The digital in-phase and quadrature tuner outputs are fed back to the digital circuit to generate the digital modulation control signal.

In another embodiment of the invention, apparatus for phase/frequency digital modulation includes a programmable logic digital circuit receiving a modulation input signal and operable to generate a modulation control signal therefrom, and an RF/analog circuit coupled to the programmable logic digital circuit and receiving the modulation control signal. The RF/analog circuit includes

a voltage controlled oscillator operable to generate a modulated output signal in response to the modulation control signal, and a quadrature tuner coupled to the voltage controlled oscillator operable to generate an in-phase tuner output and a quadrature tuner output in response to the modulation control signal. The in-phase and quadrature tuner outputs are fed back to the programmable logic digital circuit to generate the modulation control signal.

In yet another embodiment of the invention, a method for phase/frequency digital modulation includes the steps of receiving a modulation input signal and at least one feedback signal and generating a modulation control signal therefrom, using the modulation control signal to control a voltage controlled oscillator and generating a modulated output signal, generating an in-phase and a quadrature tuner outputs in response to the modulated output signal, and generating the at least one feedback signal from the in-phase and quadrature tuner outputs.

One technical advantage of the invention is that the use of the voltage controlled oscillator and quadrature feedback avoids the problems of frequency translation, digital-to-analog converter spurious and dynamic range, and high speed digital-to-analog converter drive circuitry complexity and power consumption. Another technical advantage of the invention is that identical RF/analog circuits enables the implementation of the digital circuit with programmable logic devices that can be configured.

BRIEF DESCRIPTION OF THE DRAWINGS

For a better understanding of the present invention, reference may be made to the accompanying drawings, in which:

FIGURE 1 is a block diagram of an embodiment of a narrowband phase and frequency digital modulator constructed according to the teachings of the present invention;

FIGURE 2 is a block diagram of an embodiment of a wideband phase digital modulator constructed according to the teachings of the present invention;

FIGURE 3 is a block diagram of an embodiment of a wideband frequency digital modulator constructed according to the teachings of the present invention;

FIGURE 4 is a block diagram of an embodiment of an automatic gain control circuit constructed according to the teachings of the present invention;

FIGURE 5 is a block diagram of an embodiment of a deviation calibration circuit constructed according to the teachings of the present invention;

FIGURE 6 is a flowchart of an embodiment of a method for common phase and/or frequency digital modulation according to the teachings of the present invention;

FIGURE 7 is a flowchart of an embodiment of a method for processing the modulation input signal for narrowband phase and frequency digital modulation according to the teachings of the present invention;

FIGURE 8 is a flowchart of an embodiment of a method for processing the modulation input signal for wideband phase digital modulation according to the teachings of the present invention;

FIGURE 9 is a flowchart of an embodiment of a method for processing the modulation input signal for wideband frequency digital modulation according to the teachings of the present invention;

FIGURE 10 is a flowchart of an embodiment of a method for automatic gain control loop for phase and frequency digital modulation according to the teachings of the present invention; and

FIGURE 11 is a flowchart of an embodiment of a method for generating a deviation control output signal for phase and frequency digital modulation according to the teachings of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

The preferred embodiments of the present invention are illustrated in FIGURES 1-11, where like reference numerals are used to refer to like and corresponding parts or portions of the invention.

It is important to note that certain circuit components, circuit blocks, and devices forming portions of the digital modulators of the present invention described below are well known in the art of digital signal processing. Therefore, a detailed description of the well known circuit components, circuit blocks, and devices is not required. It may also be worthwhile to note that the digital modulators of the present invention are described in the context of both algorithms and functional circuit blocks for implementing the algorithms. Therefore, the present invention anticipates any circuit designs that implement the algorithms shown in the figures and described below.

Referring to block diagrams shown in FIGURES 1-3, it may be seen that narrowband phase and frequency modulator 10 (FIGURE 1), wideband phase modulator 70 (FIGURE 2), and wideband frequency modulator 130 (FIGURE 3) each has a digital circuit portion (66, 122, 182) and a common RF/analog circuit portion 68. In general, the common phase or frequency modulator process is shown in FIGURE 6, which begins in block 230. The modulation input signal is first processed in some manner by the digital portion of the modulators, as shown in block 232. Thereafter, the processed signal is used to control a voltage controlled oscillator to generate a modulated output signal, as shown in block 238. An automatic gain control loop or process is then used to generate an output to drive an automatic gain control amplifier receiving the modulated output signal, as shown in block 242. In block 244, in-phase tuner output and quadrature tuer output are generated from the output of the automatic gain control amplifier. A feedback signal is then generated from the in-phase tuner output and/or the quadrature tuner outputs, as shown in block 246. The process ends in block 248. The process described above is relevant to each of the modulation methods described below.

A block diagram of an embodiment of a narrowband phase and frequency digital modulator 10 constructed according to the teachings of the present invention is shown in FIGURE 1. Referring also to FIGURE 7 for a flowchart of the exemplary method for narrowband phase and frequency digital modulation, which begins in block 250. A digital frequency modulation input word 12 is processed by supplying it to a phase accumulator 14, which converts input word 12 into a time varying phase representation (block 252). The output from phase accumulator 14 is summed, by a summer 17, with

a digital phase modulation input word 16 to generate a phase reference signal 18 for a modulator phase-locked loop (PLL) 20 (block 254). Phase reference signal 18 along with a feedback signal in the form of a phase signal 22 are provided to and received by a summer 19. Summer 19 subtracts phase signal 22 from phase reference signal 18 to form a phase error signal or a modulation control signal 24 (block 256) that is provided as an input to a loop filter 26. Loop filter 26 filters modulation control signal 24 (block 257). The digital portion of the process ends in block 258.

The output of loop filter 26 is a filtered modulation control signal coupled to a digital-to-analog converter (DAC) 28 followed by an anti-aliasing or low pass filter 30. The output from filter 30 drives a voltage controlled oscillator (VCO) 32 having a modulated intermediate frequency (IF) or radio frequency (RF) output 34 (FIGURE 6, block 238). When phase-locked loop 20 is locked, modulated output 34 tracks the phase of phase reference signal 18, which is modulated by frequency and phase modulation input words 12 and 16. An automatic gain control (AGC) amplifier 36 coupled to voltage controlled oscillator 32 receives modulated output 34 therefrom and generates an output with an IF/RF output power kept at a constant level (block 242). Automatic gain control amplifier 36 is driven by an output from a digital-to-analog converter 38 and low pass filter 40 combination that is connected to an output 42 of an automatic gain control loop 200 (block 238 and FIGURE 10) shown in FIGURE 4, which is described below.

Modulated IF/RF output 37 from amplifier 36 is fed back to a quadrature tuner 44 whose center frequency is controlled by an IF/RF phase-locked loop 46. The in-phase

(I) and quadrature (Q) outputs 48 and 50 of quadrature tuner 44 (block 244) are supplied to and filtered by low pass filters 52 and 54, respectively, to remove potential aliasing components. The filtered outputs from low pass filters 52 and 54 are converted to digital signals by dual analog-to-digital converters 56 and 58, respectively. The digital in-phase and quadrature signals are then provided to a coordinate transform 60, which converts the Cartesian (X, Y) in-phase and quadrature signals into polar (R, θ) amplitude and phase representations 22 and 64. Amplitude information 64 is sent to automatic gain control loop 200 (FIGURE 4) for comparison with the desired level and filtering. Phase information 22 is supplied as a feedback signal to summer 19 to be subtracted from phase reference signal 18 to generate modulation control signal 24 (block 246).

Referring to FIGURE 4, an exemplary embodiment of an automatic gain control loop 200 is shown. FIGURE 10 is a flowchart of an exemplary method for automatic gain control loop. Automatic gain control loop 200 includes a summer 202 for subtracting amplitude information (AGC input) 64 received from coordinate transform 60 (FIGURE 1) from an automatic gain control reference signal. In effect, summer 202 obtains a difference or a comparison of amplitude information 64 and the automatic gain control reference signal (block 312) to generate a result signal (block 314). The automatic gain control reference signal may be a predetermined fixed signal or one generated by a known method or process executed by a microprocessor, computer, or other computing platforms. The output from summer 202 is supplied to an integrator 204. The output of integrator 204 or automatic gain control loop 200 is coupled to

digital-to-analog converter 38 (FIGURE 1), having an output that is low pass filtered and used to control automatic gain control amplifier 36 (block 316). The process then returns to block 244 in FIGURE 6 (block 318).

In this manner, amplitude information 64 is used as a feedback signal for automatic gain control loop 200 and phase information 22 is used as a feedback signal for modulator phase-locked loop 20.

An advantage of the present invention is that modulation deviation is accurate, since it is directly controlled by a digital source.

Referring to FIGURE 2, a block diagram of an embodiment of a wideband phase modulator 70 is shown according to the present invention. Reference is also made to flowcharts shown in FIGURES 6, 8, 10, and 11. The process begins in the flowchart shown in FIGURE 6, with the flowchart shown in FIGURE 8 supplying details on an embodiment of wideband phase digital modulation signal processing (block 270) according to the present invention. The flowcharts in FIGURES 10 and 11 supply details on automatic gain control and deviation signal generating processes, respectively.

Referring first to FIGURE 6, the modulation input signal is received and processed (block 232) to remove noise and signals residing in certain frequencies, for example. A digital phase modulation input word 72 is supplied to a bandpass filter 74 (FIGURE 8, block 272) having an input coupled to a multiplier 78. Low input frequencies are rejected by bandpass filter 74 to prevent interference with the operation of modulator 70. High frequencies which cannot be processed accurately by a finite impulse response (FIR) differentiator 76 coupled to

the output of multiplier 78 are also rejected by bandpass filter 74. The bandpass filter output is also routed to a deviation calibration loop 210 (FIGURE 5) or function 320 (FIGURE 11), to be described. Deviation calibration loop 210 and function 320 essentially compare the filtered phase modulation input signal 72 and phase signal 118 generated by coordinate transform 116 (block 274) to generate a deviation control signal 80 (block 276). Deviation calibration multiplier 78 uses deviation control signal 80 to adjust the filtered phase modulation input signal to produce the required phase modulation peak deviation (block 278). The output of multiplier 78 is coupled to finite impulse response differentiator 76, which differentiates the multiplier output (block 280). The finite impulse response differentiator output is then summed with the output of a modulator loop filter 84 by a summer 85 (block 284). The input to modulator loop filter 84 is phase signal 118 from coordinate transform 116 (block 282). The process shown in FIGURE 8 ends in block 286.

The processed phase modulation input signal and a feedback signal consisting of the filtered phase signal from loop filter 84 are received at summer 85 (block 234) to generate a modulation control signal 86 (block 236). Modulation control signal 86 is then converted into analog form by a digital-to-analog converter 88 and then filtered (block 237), by a lowpass filter 90, for example. The output from lowpass filter 90 is provided to a voltage controlled oscillator 92, which generates a modulated output signal (block 238). An automatic gain control amplifier 94 is coupled to voltage controlled oscillator 92 to keep the output power of the modulated output signal at a constant level. Automatic gain control amplifier 94 is

driven by an output from a digital-to-analog converter 96 and lowpass filter 98 that are coupled to an output 100 of an automatic gain control loop 200 (block 240), an embodiment of which is shown in FIGURES 4 and 10 as described.

It may be seen that in operation, finite impulse response differentiator 76 produces a signal that is used to tune voltage controlled oscillator 92 to produce phase modulation. Finite impulse response differentiator 76 may also provide compensation to correct amplitude vs. frequency nonlinearities in digital-to-analog converter 88, lowpass filter 90, and/or voltage controlled oscillator 92.

IF/RF modulated output 102 from amplifier 94 is fed back to a quadrature tuner 104 whose center frequency is controlled by an IF/RF phase-locked loop 106 (block 244). The in-phase and quadrature outputs of quadrature tuner 104 are filtered to remove potential aliasing components by, for example, lowpass filters 108 and 110, respectively, and then converted to digital form by dual analog-to-digital converters 112 and 114, respectively (block 246). A coordinate transform 116 receives and converts the digital in-phase and quadrature signals into phase and amplitude representations 118 and 120 (block 246). Amplitude information 120 is provided to an automatic gain control loop (an embodiment 200 shown in FIGURE 4) for comparison with the desired reference level and filtering.

Phase information 118 from coordinate transform 116 is provided to modulator phase-lock loop filter 84, the output of which is summed with the feed-forward modulation signal from finite impulse response differentiator 76. Phase information 118 is also provided to deviation calibration loop 210 (FIGURE 5).

Referring to FIGURE 5, an embodiment of a deviation calibration loop 210 is shown, and to FIGURE 11, a flowchart of the process for generating a deviaiton output signal is shown. Deviation calibration loop 210 includes a squarer 212 receiving measured phase information 118 from coordinate transform 116 and a squarer 214 receiving the filtered phase modulation input signal from bandpass filter 74 (blocks 322 and 324). The squared values are supplied to a summer 216, which subtracts the squared measured phase information 118 from the squared filtered phase modulation input (block 326). The output from summer 216 is coupled to an integrator 218 (block 328), which generates a deviation control output (block 330). The process ends in block 332.

In operation, the mean square values of the measured phase information 118 and the filtered phase modulation input are compared. The comparison output is filtered by integrator 218, which generates a deviation control signal 80 that is supplied to multiplier 78 (FIGURE 2).

Note that wideband PM modulator 70 may be divided into a digital portion 122 and the same RF/analog portion 68 as that of narrowband PM/FM modulator 10 shown in FIGURE 1. Further, it may be noted that the RF/analog portions of modulators 10 and 70 are the same.

A block diagram of an embodiment of a wideband frequency modulator 130 is shown in FIGURE 3. Flowcharts of processes of frequency modulation are shown in FIGURES 6, 9, 10 and 11. FIGURE 9, in particular, shows a flowchart of an embodiment of frequency modulation input signal processing 290. Referring to FIGURE 3 and 6, a frequency modulation input word 132 is received and processed (block 232) by filtering with a highpass filter 134 to eliminate

low input frequencies which may interfere with the operation of modulator loop (FIGURE 9, block 292). The highpass filter output is then routed to a requested deviation input of a deviation calibration loop 210, such as the one shown in FIGURE 5 and described above. The deviation calibration process 320 is also shown in FIGURE 11 and basically compares the filtered frequency modulation input signal with the frequency signal derived from the phase signal output from a coordinate transform 174 (block 296). The deviation calibration loop and process generate a deviation control signal 138 (block 298). A deviation calibration multiplier 136 uses deviation control signal 138 to adjust the filtered frequency modulation input signal from highpass filter 134 to produce the required frequency modulation peak deviation (block 300). The multiplier output is then provided to a summer 137, which sums it with the output from a modulator loop filter 140 to generate a modulation control signal 142 (blocks 302 and 304). Process 290 ends in block 306.

Modulation control signal 142 is converted into analog form by a digital-to-analog converter 144 and then provided to a lowpass filter 146 (FIGURE 6, block 238). The lowpass filter output controls a voltage controlled oscillator 148, which generates a modulated output signal 150 (block 238). An automatic gain control amplifier 152 is coupled to the output of voltage controlled oscillator 148 to keep the output power of output signal 150 at a substantially constant level and generates a modulated output signal 154 therefrom. Automatic gain control amplifier 152 is driven by a digital-to-analog converter 156 coupled in series with a lowpass filter 158, which are in turn coupled to an output 160 of an automatic gain control loop (block 240),

an embodiment is shown in FIGURE 4. The automatic gain control process is also shown in FIGURE 10.

IF/RF modulated output signal 154 is fed back to a quadrature tuner 162 whose center frequency is controlled by an IF/RF phase-locked loop 164 (block 244). The in-phase and quadrature outputs of quadrature tuner 162 are filtered by lowpass filters 166 and 168, respectively, to remove potential aliasing components, then converted to digital form by dual analog-to-digital converters 170 and 172, respectively. A coordinate transform 174 coupled to analog-to-digital converters 170 and 172 converts the digital in-phase and quadrature outputs into polar phase and amplitude representations 176 and 178 thereof (block 246). Amplitude information 178 is provided to the automatic gain control loop for comparison with the desired level and filtering (FIGURE 10, block 312).

Phase information 176 is provided to modulator phase-locked loop filter 140, the output of which is then summed with the feed-forward modulation signal from multiplier 136. Phase information 176 is also provided to a backward difference circuit or input-previous circuit 180 to obtain frequency information. Input-previous block provides a difference between the current phase information and a previous phase information. The measured feedback frequency from backward difference circuit 180 is then provided to the deviation calibration loop, which compares the filtered frequency modulation input signal mean square value with the measured frequency deviation mean square value (FIGURE 9, block 296). The comparison output is then supplied to a integrator 218 (FIGURE 5 and FIGURE 11, block 328), which generates deviation control signal 138 (blocks 298 and 330). The deviation control signal is provided to

multiplier 136 and is multiplied thereby with the filtered frequency modulation input signal (block 300) to generate the modulation control signal (FIGURE 6, block 236).

Note that wideband frequency modulator 130 may be divided into a digital portion 182 and the same RF/analog portion 68 as that of narrowband PM/FM modulator 10 shown in FIGURE 1 and wideband phase modulator 70 shown in FIGURE 2.

The embodiments of the present invention shown in FIGURES 1-11 use a voltage controlled oscillator and quadrature tuner feedback to address the problems of frequency translation, digital analog converter spurious and dynamic range, and high speed digital-to-analog converter drive circuitry complexity and power. In addition, all three embodiments include an identical RF/analog section 68. Therefore, implementation of the digital portions 66, 122, and 182 of these digital modulators with programmable logic devices would allow configuration of any of these modulators on a single platform.

Although several embodiments of the present invention and its advantages have been described in detail, it should be understood that mutations, changes, substitutions, transformations, modifications, variations, and alterations can be made therein without departing from the teachings of the present invention, the spirit and scope of the invention being set forth by the appended claims.

WHAT IS CLAIMED IS:

1. Apparatus for phase/frequency digital modulation, comprising:

a digital circuit receiving and processing a digital modulation input signal to generate a digital modulation control signal;

a digital-to-analog converter coupled to the digital circuit for converting the digital modulation control signal into an analog modulation control signal; and

an RF/analog circuit coupled to the digital-to-analog converter, the RF/analog circuit comprising:

a voltage controlled oscillator generating a modulated output signal in response to the analog modulation control signal;

a quadrature tuner coupled to the voltage controlled oscillator generates an in-phase tuner output and a quadrature tuner output in response to the modulated output signal; and

two analog-to-digital converters coupled to the quadrature tuner convert the in-phase and quadrature tuner outputs to digital in-phase and quadrature tuner outputs, the digital in-phase and quadrature tuner outputs being fed back to the digital circuit to generate the digital modulation control signal.

2. The apparatus, as set forth in claim 1, wherein the RF/analog circuit further comprises two filters coupled to the quadrature tuner to filter aliasing components from the in-phase and quadrature tuner outputs.

3. The apparatus, as set forth in claim 1, wherein the RF/analog circuit further comprises an automatic gain control amplifier coupled to the voltage controlled oscillator to maintain the power of the modulated output signal substantially at a predetermined level.

4. The apparatus, as set forth in claim 1, wherein the RF/analog circuit further comprises a lowpass filter coupled to the digital-to-analog converter for filtering aliasing components from the analog modulation control signal to generate a filtered analog modulation control signal provided to the voltage controlled oscillator.

5. The apparatus, as set forth in claim 1, wherein the digital circuit comprises a coordinate transformer coupled to the analog-to-digital converter for converting the in-phase and quadrature tuner outputs to phase and amplitude signals.

6. The apparatus, as set forth in claim 5, wherein the digital circuit comprises:

a phase accumulator receiving a digital frequency modulation input signal and converting the digital frequency modulation signal into a time varying phase signal;

a first summer coupled to the phase accumulator for summing the time varying phase signal and a digital phase modulation input signal to generate a phase reference signal; and

a second summer coupled to the first summer and the coordinate transformer and to subtract the phase signal from the phase reference signal; and

a filter coupled to the second summer generating the digital modulation control signal supplied to the digital-to-analog converter.

7. The apparatus, as set forth in claim 5, further comprising:

an automatic gain control amplifier coupled to the voltage controlled oscillator to maintain the power level of the modulated output signal substantially constant;

an automatic gain control loop coupled to the coordinate transformer to compare the amplitude signal therefrom with a reference signal and generate a result signal to drive the automatic gain control amplifier.

8. The apparatus, as set forth in claim 5, wherein the digital circuit comprises:

a deviation calibration loop receiving a digital phase modulation input signal and the phase signal from the coordinate transformer to compare the digital phase modulation input signal and the phase signal to generate a deviation control output;

a multiplier coupled to the deviation calibration loop to multiply the digital phase modulation input signal by the deviation control output to generate a multiplier output; and

a summer coupled to the multiplier and the coordinate transformer to receive and sum the multiplier output and the phase signal to generate the digital modulation control signal supplied to the digital-to-analog converter.

9. The apparatus, as set forth in claim 8, wherein the digital circuit further comprises a bandpass filter receiving the digital phase modulation input signal and generating a filtered digital phase modulation input signal supplied to the deviation calibration loop and the multiplier.

10. The apparatus, as set forth in claim 8, wherein the digital circuit further comprises a finite impulse response differentiator coupled to the output of the multiplier to generate a differentiated multiplier output supplied to the summer.

11. The apparatus, as set forth in claim 8, wherein the digital circuit further comprises a filter coupled to the coordinate transform to receive the phase signal therefrom and generate a filtered phase signal supplied to the summer.

12. The apparatus, as set forth in claim 11, wherein the deviation calibration loop comprises:

a first squarer receiving the filtered digital phase modulation input signal from the bandpass filter and generating a squared phase modulation input signal;

a second squarer receiving the phase signal from the coordinate transform to generate a squared phase signal;

a second summer coupled to the first and second squarers to receive and compare the squared phase signal and the squared phase modulation input signal to generate a comparison signal; and

a deviation loop filter coupled to the second summer to generate the deviation control output.

13. The apparatus, as set forth in claim 5, wherein the digital circuit comprises:

a backward difference circuit coupled to the coordinate transformer and generating a frequency signal from the phase signal therefrom;

a deviation calibration loop receiving and comparing a digital frequency modulation input signal and the frequency signal to generate a deviation output in response thereto;

a multiplier coupled to the deviation calibration loop to multiply the digital frequency modulation input signal by the deviation output to generate a multiplier output; and

a summer coupled to the multiplier and the coordinate transformer to receive and sum the multiplier output and the phase signal to generate the digital modulation control signal provided to the digital-to-analog converter.

14. The apparatus, as set forth in claim 13, wherein the digital circuit further comprises a highpass filter receiving the digital frequency modulation input signal to generate a filtered digital frequency modulation input signal supplied to the deviation calibration loop.

15. The apparatus, as set forth in claim 13, wherein the digital circuit further comprises a filter coupled to the coordinate transformer to receive the phase signal therefrom and generate a filtered phase signal supplied to the summer.

16. The apparatus, as set forth in claim 14, wherein the deviation calibration loop comprises:

a first squarer receiving the filtered digital frequency modulation input signal from the highpass filter and generating a squared frequency modulation input signal;

a second squarer receiving the frequency signal from the backward difference circuit to generate a squared frequency signal;

a second summer coupled to the first and second squarers to receive and compare the squared frequency signal and the squared frequency modulation input signal to generate a comparison signal; and

a filter coupled to the second summer to generate the deviation control output.

17. Apparatus for phase/frequency digital modulation, comprising:

a programmable logic digital circuit receiving a modulation input signal and generating a modulation control signal; and

an RF/analog circuit coupled to the programmable logic digital circuit and receiving the modulation control signal, the RF/analog circuit comprising:

a voltage controlled oscillator generating a modulated output signal in response to the modulation control signal; and

a quadrature tuner coupled to the voltage controlled oscillator to generate an in-phase tuner output and a quadrature tuner output in response to the modulation control signal, the in-phase and quadrature tuner outputs being fed back to the programmable logic digital circuit to generate the modulation control signal.

18. The apparatus, as set forth in claim 17, wherein the RF/analog circuit further comprises two filters coupled to the quadrature tuner to filter aliasing components from the in-phase and quadrature tuner outputs.

19. The apparatus, as set forth in claim 17, wherein the digital circuit comprises a coordinate transform coupled to the quadrature tuner to convert the in-phase and quadrature tuner outputs to phase and amplitude signals.

20. The apparatus, as set forth in claim 17, wherein the RF/analog circuit further comprises an automatic gain control amplifier coupled to the voltage controlled oscillator to maintain the power level of the modulated output signal substantially constant.

21. The apparatus, as set forth in claim 19, wherein the programmable logic digital circuit comprises:

a phase accumulator receiving a frequency modulation input signal and converting the frequency modulation signal into a time varying phase signal;

a first summer coupled to the phase accumulator to receive and sum the time varying phase signal and a phase modulation input signal to generate a phase reference signal; and

a second summer coupled to the first summer and the coordinate transformer to subtract the phase signal from the phase reference signal; and

a loop filter coupled to the second summer generating the modulation control signal supplied to the voltage controlled oscillator.

22. The apparatus, as set forth in claim 17, wherein the RF/analog circuit further comprises a lowpass filter coupled to the programmable logic digital circuit to filter aliasing components from the modulation control signal to generate a filtered modulation control signal provided to the voltage controlled oscillator.

23. The apparatus, as set forth in claim 17, further comprising:

an automatic gain control amplifier coupled to the voltage controlled oscillator to maintain the power level of the modulated output signal substantially constant; and

an automatic gain control loop coupled to the coordinate transform to compare the amplitude signal output with a reference signal and generate a result signal to drive the automatic gain control amplifier.

24. The apparatus, as set forth in claim 19, wherein the programmable logic digital circuit comprises:

a deviation calibration loop receiving a phase modulation input signal and the phase signal from the coordinate transformer to compare the phase modulation input signal and the phase signal to generate a deviation control output;

a multiplier coupled to the deviation calibration loop to multiply the phase modulation input signal by the deviation control output to generate a multiplier output; and

a summer coupled to the multiplier and the coordinate transformer to receive and sum the multiplier output and the phase signal to generate the modulation control signal.

25. The apparatus, as set forth in claim 24, wherein the programmable logic digital circuit further comprises a bandpass filter receiving the phase modulation input signal and generating a filtered phase modulation input signal supplied to the deviation calibration loop and the multiplier.

26. The apparatus, as set forth in claim 24, wherein the programmable logic digital circuit further comprises a finite impulse response differentiator coupled to the output of the multiplier to generate a differentiated multiplier output supplied to the summer.

27. The apparatus, as set forth in claim 24, wherein the programmable logic digital circuit further comprises a filter coupled to the coordinate transformer to receive the phase signal and generate a filtered phase signal supplied to the summer.

28. The apparatus, as set forth in claim 25, wherein the deviation calibration loop comprises:

a first squarer receiving the filtered phase modulation input signal from the bandpass filter to generate a squared phase modulation input signal;

a second squarer receiving the phase signal from the coordinate transformer to generate a squared phase signal;

a second summer coupled to the first and second squarers to receive and compare the squared phase signal and the squared phase modulation input signal to generate a comparison signal; and

a deviation loop filter coupled to the second summer to generate the deviation output.

29. The apparatus, as set forth in claim 19, wherein the programmable logic digital circuit comprises:

a backward difference circuit coupled to the coordinate transformer to generate a frequency signal from the phase signal therefrom;

a deviation calibration loop receiving a digital frequency modulation input signal and the frequency signal to compare the digital frequency modulation input signal and the frequency signal to generate a deviation output;

a multiplier coupled to the deviation calibration loop to multiply the frequency modulation input signal by the deviation output to generate a multiplier output; and

a summer coupled to the multiplier and the coordinate transformer to receive and sum the multiplier output and the phase signal to generate the modulation control signal provided to the voltage controlled oscillator.

30. The apparatus, as set forth in claim 29, wherein the programmable logic digital circuit further comprises a highpass filter receiving the digital frequency modulation input signal to generate a filtered frequency modulation input signal supplied to the deviation calibration loop and the multiplier.

31. The apparatus, as set forth in claim 29, wherein the programmable logic digital circuit further comprises a filter coupled to the coordinate transformer to receive the phase signal and generate a filtered phase signal supplied to the summer.

32. The apparatus, as set forth in claim 30, wherein the deviation calibration loop comprises:

a first squarer receiving the filtered frequency modulation input signal from the highpass filter and generating a squared frequency modulation input signal;

a second squarer receiving the frequency signal from the backward difference circuit to generate a squared frequency signal;

a second summer coupled to the first and second squarers to receive and compare the squared frequency signal and the squared frequency modulation input signal to generate a comparison signal; and

a deviation loop filter coupled to the second summer to generate the deviation output.

33. A method for phase/frequency digital modulation, comprising:

receiving a modulation input signal and at least one feedback signal and generating a modulation control signal;

controlling a voltage controlled oscillator in response to the modulation control signal and generating a modulated output signal;

generating an in-phase tuner output and a quadrature tuner output in response to the modulated output signal; and

generating the at least one feedback signal from the in-phase tuner output and quadrature tuner output.

34. The method, as set forth in claim 33, further comprising filtering aliasing components from the in-phase tuner output and quadrature tuner output.

35. The method, as set forth in claim 33, further comprising transforming the coordinates of the in-phase tuner output and quadrature tuner output to a phase signal and an amplitude signal.

36. The method, as set forth in claim 33, further comprising maintaining the power level of the modulated output signal substantially constant.

37. The method, as set forth in claim 35, wherein receiving a modulation input signal further comprises:

converting the frequency modulation input signal into a time varying phase signal;

summing the time varying phase signal and a digital phase modulation input signal and generating a phase reference signal; and

subtracting the phase signal from the phase reference signal and generating the modulation control signal.

38. The method, as set forth in claim 33, further comprising removing aliasing components from the modulation control signal and generating a filtered modulation control signal to generate the modulated output signal.

39. The method, as set forth in claim 33, further comprising:

comparing an amplitude signal with a reference signal and generating a result signal; and

controlling the power level of the modulated output signal substantially constant in response to the result signal.

40. The method, as set forth in claim 33, further comprising:

comparing a phase modulation input signal and the phase signal and generating a deviation output;

multiplying the phase modulation input signal by the deviation output and generating a multiplier output;

differentiating the multiplier output and generating a differentiated multiplier output; and

summing the differentiated multiplier output and the phase signal and generating the modulation control signal.

41. The method, as set forth in claim 40, further comprising:

bandpass filtering the phase modulation input signal and generating a filtered phase modulation input signal; and

generating the deviation output in response to the filtered phase modulation input signal.

42. The method, as set forth in claim 40, summing further comprising filtering the phase signal and generating a filtered phase signal to be summed with the differentiated multiplier output to generate the modulation control signal.

43. The method, as set forth in claim 41, further comprising:

squaring the filtered phase modulation input signal and generating a squared phase modulation input signal;

squaring the phase signal and generating a squared phase signal;

summing the squared phase signal and the squared phase modulation input signal to generate a comparison signal; and

filtering the comparison signal and generating the deviation output in response thereto.

44. The method, as set forth in claim 35, further comprising:

generating a frequency signal from the phase signal;

comparing a frequency modulation input signal and the frequency signal to generate a deviation output;

multiplying the frequency modulation input signal by the deviation output to generate a multiplier output; and

summing the multiplier output and the phase signal to generate the modulation control signal.

45. The method, as set forth in claim 44, further comprising highpass filtering the frequency modulation input signal and generating a filtered frequency modulation input signal.

46. The method, as set forth in claim 44, further comprising filtering the phase signal and generate a filtered phase signal to be summed with the multiplier output to generate the modulation control signal.

47. The method, as set forth in claim 44, further comprising:

squaring the filtered frequency modulation input signal and generating a squared frequency modulation input signal;

squaring the frequency signal and generating a squared frequency signal;

summing the squared frequency signal and the squared frequency modulation input signal and generating a comparison signal thereof; and

filtering the comparison signal and generating the deviation output.

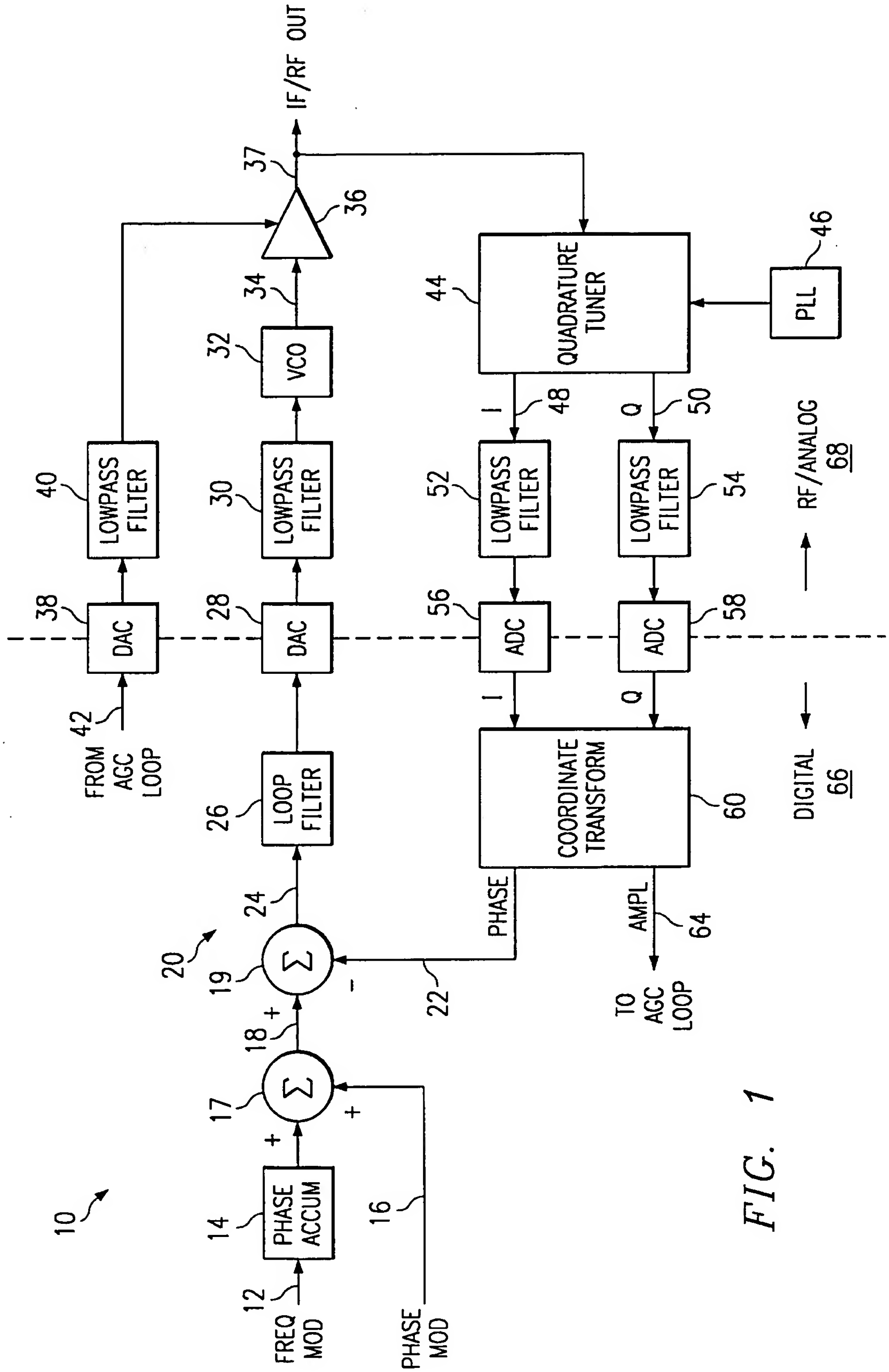

10
FREQ MOD
12
PHASE ACCUM
14
PHASE MOD
16
17
18
19
20
22
24
LOOP FILTER
26
DAC
28
LOWPASS FILTER
30
VCO
32
34
36
37
IF/RF OUT
FROM AGC LOOP
42
DAC
38
LOWPASS FILTER
40
QUADRATURE TUNER
44
PLL
46
I
48
Q
50
LOWPASS FILTER
52
LOWPASS FILTER
54
ADC
56
ADC
58
COORDINATE TRANSFORM
60
PHASE
AMPL
64
TO AGC LOOP
DIGITAL
66
RF/ANALOG
68

FIG. 1

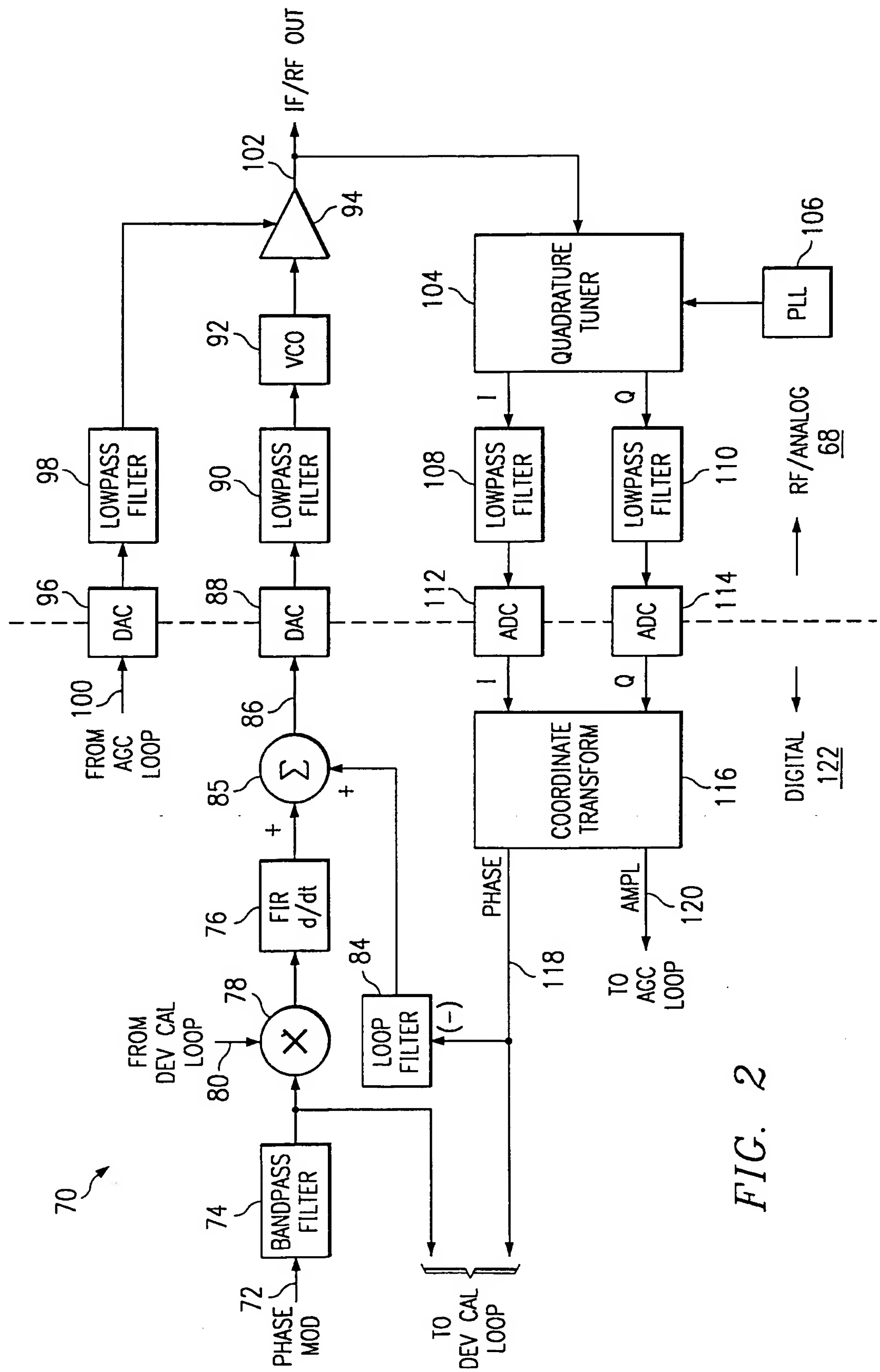

IF/RF OUT
102
94
98
LOWPASS FILTER
92
VCO
90
LOWPASS FILTER
104
QUADRATURE TUNER
106
PLL
I
Q
108
LOWPASS FILTER
110
LOWPASS FILTER
96
DAC
88
DAC
112
ADC
114
ADC
RF/ANALOG
68
100
FROM AGC LOOP
86
I
Q
85
Σ
+
+
COORDINATE TRANSFORM
116
DIGITAL
122
76
FIR d/dt
PHASE
AMPL
120
84
118
TO AGC LOOP
78
FROM DEV CAL LOOP
80
LOOP FILTER
(-)
70
74
BANDPASS FILTER
72
PHASE MOD
TO DEV CAL LOOP

FIG. 2

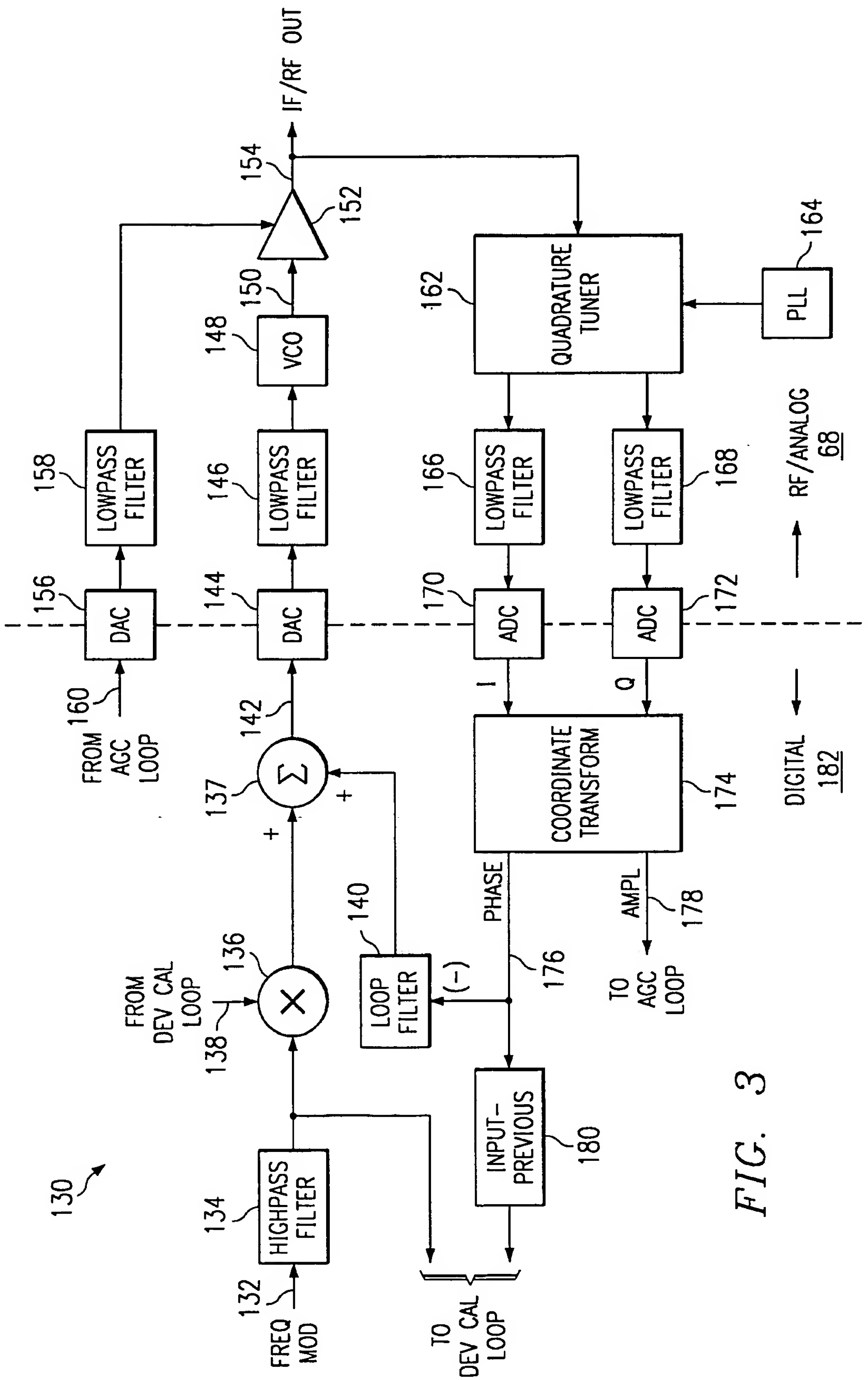

IF/RF OUT
154
152
158
LOWPASS FILTER
146
LOWPASS FILTER
148
VCO
150
162
QUADRATURE TUNER
164
PLL
166
LOWPASS FILTER
168
LOWPASS FILTER
RF/ANALOG
68
156
DAC
144
DAC
170
ADC
172
ADC
160
FROM AGC LOOP
142
I
Q
DIGITAL
182
137
Σ
+
+
COORDINATE TRANSFORM
174
PHASE
AMPL
178
140
LOOP FILTER
(−)
176
TO AGC LOOP
136
FROM DEV CAL LOOP
138
130
134
HIGHPASS FILTER
132
FREQ MOD
INPUT–PREVIOUS
180
TO DEV CAL LOOP

FIG. 3

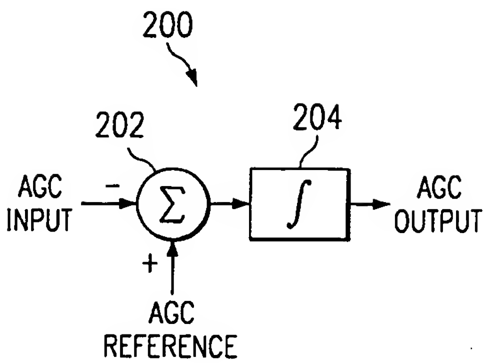


FIG. 4

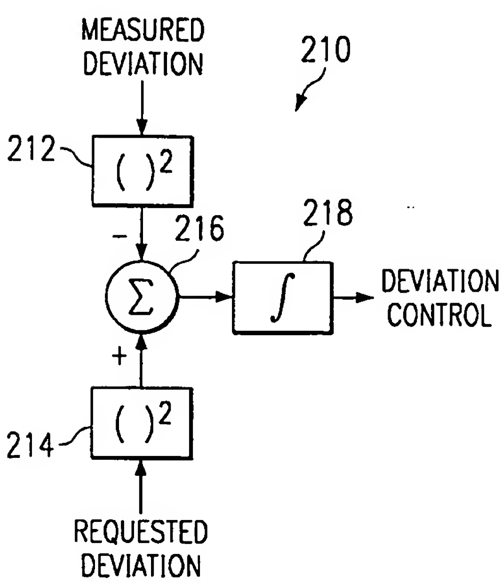


FIG. 5

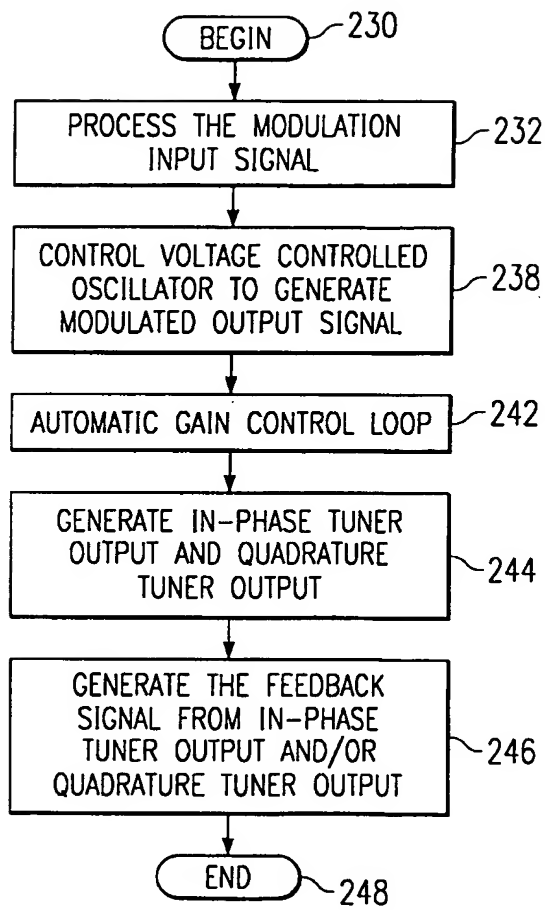


FIG. 6

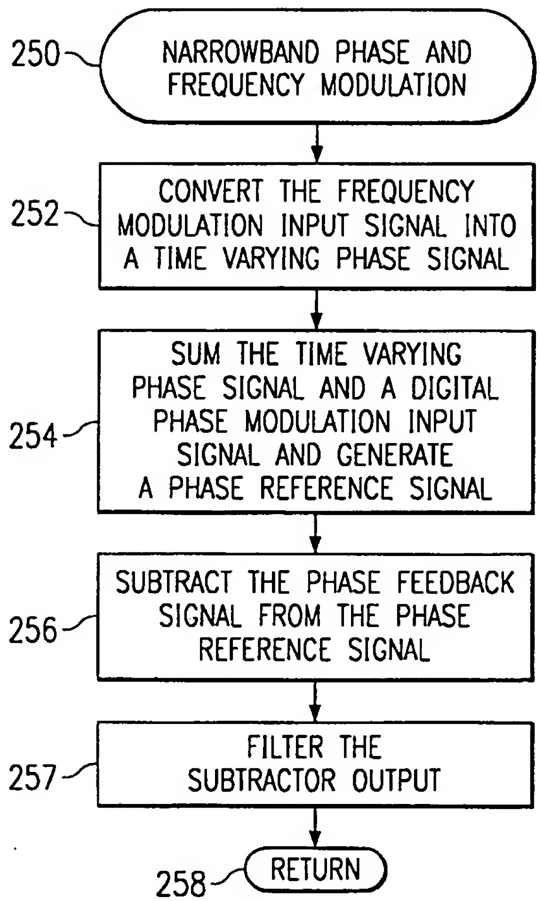

250
NARROWBAND PHASE AND FREQUENCY MODULATION
252
CONVERT THE FREQUENCY MODULATION INPUT SIGNAL INTO A TIME VARYING PHASE SIGNAL
254
SUM THE TIME VARYING PHASE SIGNAL AND A DIGITAL PHASE MODULATION INPUT SIGNAL AND GENERATE A PHASE REFERENCE SIGNAL
256
SUBTRACT THE PHASE FEEDBACK SIGNAL FROM THE PHASE REFERENCE SIGNAL
257
FILTER THE SUBTRACTOR OUTPUT
258
RETURN

FIG. 7

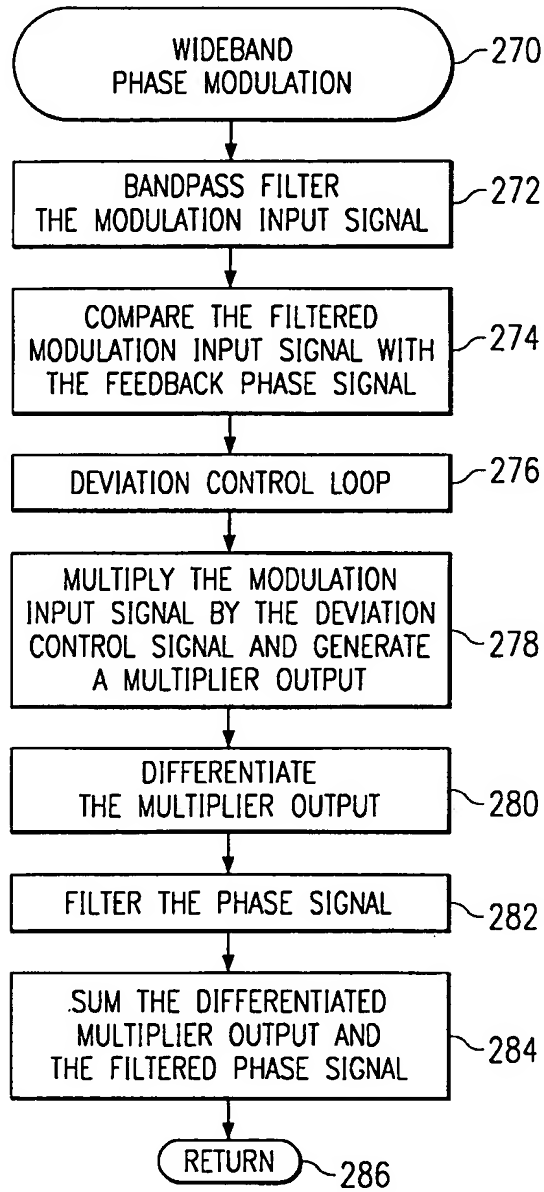

WIDEBAND PHASE MODULATION
270
BANDPASS FILTER THE MODULATION INPUT SIGNAL
272
COMPARE THE FILTERED MODULATION INPUT SIGNAL WITH THE FEEDBACK PHASE SIGNAL
274
DEVIATION CONTROL LOOP
276
MULTIPLY THE MODULATION INPUT SIGNAL BY THE DEVIATION CONTROL SIGNAL AND GENERATE A MULTIPLIER OUTPUT
278
DIFFERENTIATE THE MULTIPLIER OUTPUT
280
FILTER THE PHASE SIGNAL
282
SUM THE DIFFERENTIATED MULTIPLIER OUTPUT AND THE FILTERED PHASE SIGNAL
284
RETURN
286

FIG. 8

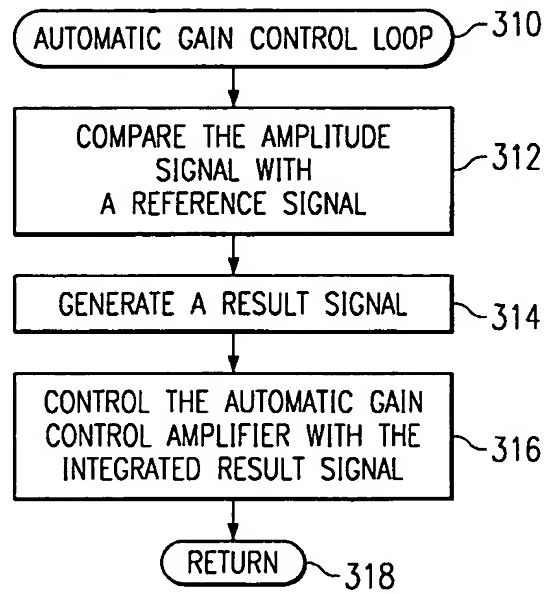


FIG. 10

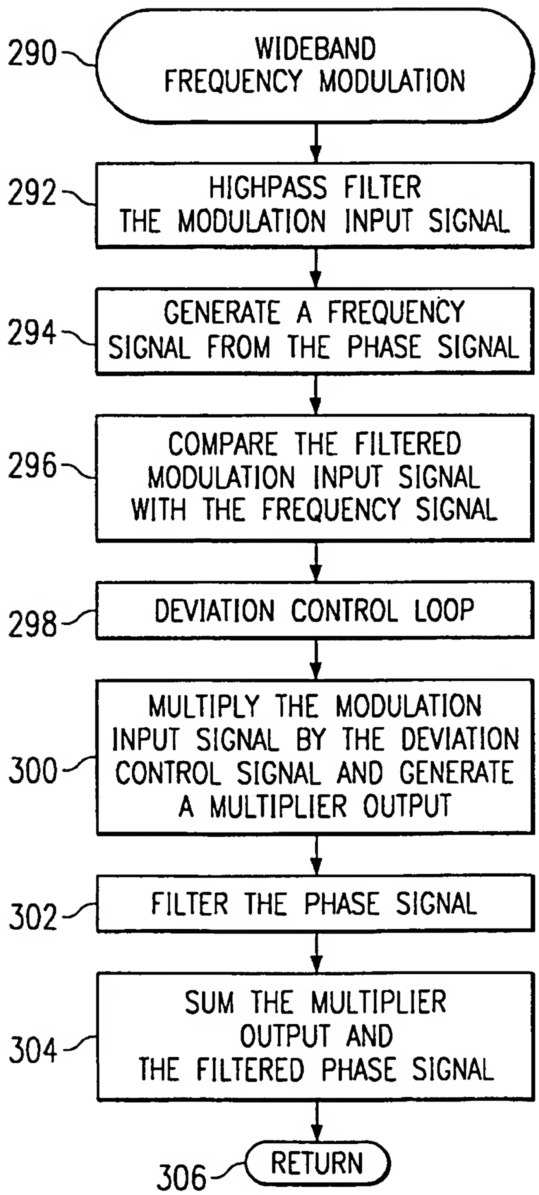


FIG. 9

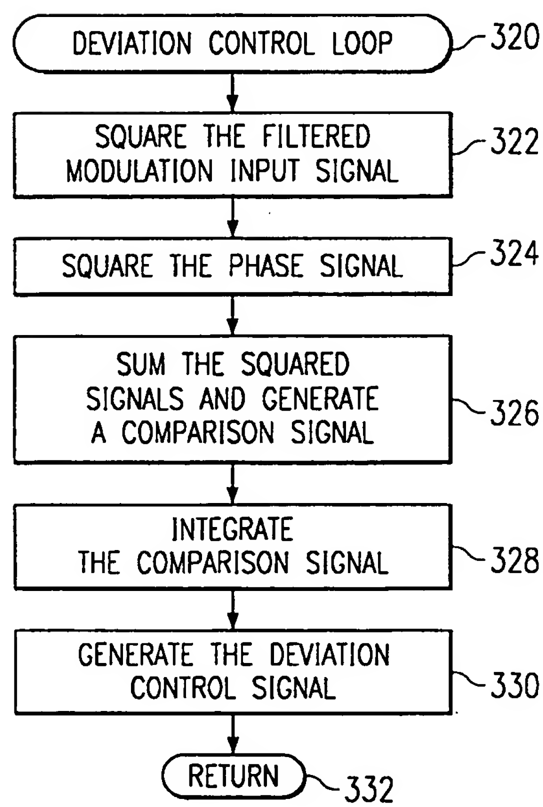


FIG. 11

INTERNATIONAL SEARCH REPORT

Interne   al Application No
PCT/US 00/21016

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H03C3/09

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H03C H03L H04L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 894 592 A (D. BRUESKE) 13 April 1999 (1999-04-13) column 2, line 33 -column 3, line 24; figure 2 ---	17,33
A	US 5 697 068 A (R. SALVI) 9 December 1997 (1997-12-09) column 4, line 10 -column 4, line 44; figures 2,3 ---	1
A	US 5 027 087 A (A. RITTINGHAUS) 25 June 1991 (1991-06-25) column 1, line 57 -column 3, line 23; figures 1,2 ---	1

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
9 November 2000	15/11/2000

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Butler, N

1

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Interna   al Application No
PCT/US 00/21016

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	US 5 483 203 A (A. ROTTINGHAUS) 9 January 1996 (1996-01-09) column 2, line 62 -column 3, line 63; figure 1 ---	1
A	EP 0 889 595 A (SIEMENS AG.) 7 January 1999 (1999-01-07) claim 1; figure 1 -----	1

1

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/US 00/21016

Patent document cited in search report		Publication date	Patent family member(s)			Publication date
US 5894592	A	13-04-1999	NONE			
US 5697068	A	09-12-1997	NONE			
US 5027087	A	25-06-1991	AU	633228	B	21-01-1993
			AU	8851891	A	21-08-1991
			CA	2049346	A,C	03-08-1991
			EP	0440449	A	07-08-1991
			JP	4506737	T	19-11-1992
			KR	9505159	B	19-05-1995
			WO	9111852	A	08-08-1991
US 5483203	A	09-01-1996	AU	3638995	A	23-05-1996
			WO	9613895	A	09-05-1996
EP 889595	A	07-01-1999	DE	19727810	C	18-02-1999
			JP	11068558	A	09-03-1999
			US	6046643	A	04-04-2000